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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/476,622    12/31/99    CHIN

H    884.101US1

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TM02/0927

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EXAMINER

TREAT. IN

ART UNIT	PAPER NUMBER
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2183

DATE MAILED:

5

09/27/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

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# Office Action Summary

Application No.

09/476,622

Applicant(s)

Chin et al.

Examiner

W. TREAT

Group Art Unit

2183

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

## Status

- ☒ Responsive to communication(s) filed on 12/31/99
- ☐ This action is FINAL.
- ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- ☒ Claim(s) 1-20 is/are pending in the application.
- Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- ☒ Claim(s) 1-20 is/are rejected.
- ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- ☐ Claim(s) \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119 (a)-(d)

- ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- ☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been received.
- ☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_.
- ☐ received in this national stage application from the International Bureau (PCT Rule 1.7.2(a)).

\*Certified copies not received: \_\_\_\_\_

## Attachment(s)

- ☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4
- ☐ Interview Summary, PTO-413
- ☒ Notice of Reference(s) Cited, PTO-892
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Other \_\_\_\_\_

Office Action Summary

1. Claims 1-20 are presented for examination.
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hotta et al. (Patent No. 5,274,829).
4. The examiner would recommend applicants review Fig. 2, col. 4, line 10 through col. 5, line 10, and col. 10, lines 21-30, at a minimum, before responding.
5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each

claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hotta et al. (Patent No. 5,274,829).

6. Hotta taught the invention of claim 1 from which claim 3 depends (see paragraphs 3-4, *supra*. While Hotta taught storing the microcode in external memory (2001), he taught this external memory as semiconductor memory and not as a mass storage device. However, the examiner takes Official Notice of three facts:

(a) A mass storage device is just another element of the basic memory hierarchy of computers. One stores data and instructions throughout the hierarchy based on the criticality of the need for the data or instructions (i.e., the most critical data and instructions being stored in the closest and most quickly accessed forms of memory such as internal registers, internal RAM, internal ROM, etc. and less critical data and instructions being stored in more remote and less quickly accessed forms of memory such as external semiconductor memory followed by forms such as hard drives, floppy disks, magnetic tape, etc.).

(b) Cost of memory per bit and technological limitations may also guide one of ordinary skill in deciding how much memory of a given type to provide and

therefore affect where data and instructions are stored.

(c) Finally, various copies of data and instructions located in various forms of memory may be provided by one of ordinary skill to provide redundancy and/or reconfigurability.

Applicants' claim 3 is nothing more than application of these basic principles of computer design to their invention (i.e. they have stored the microcode on a mass storage device because the microcode is less critical than other microcode, or the price target for the device has forced less critical data to the mass storage device, or applicants have done so for purposes of redundancy or reconfigurability. Such commonplace design choices do not represent patentability.

7. Claims 9 and 13-14 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Demers et al. (WO 94/12929).

8. The examiner would recommend applicants read page 8, line 25 through page 9, line 3 before responding.

9. Claims 1-2, 15 and 17 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Dao et al. (Patent No. 4,928,223).

10. The examiner would recommend applicants read col. 24, line 37 through col. 27, line 3 before responding.

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dao et al. (Patent No. 4,923,223).

12. Dao taught the invention of claim 15 from which claim 17 depends (see paragraphs 9-10, *supra*. The examiner considers Dao's teaching of RAM storing microcode which can be downloaded from main memory according to the nature of the task currently in execution (col. 25, lines 58-66) to be modifiable firmware to the extent claimed by applicants. However, the examiner also takes Official Notice of the fact that advances in the art related to programmable read only memory such as EEPROM, flash memory, etc. have resulted in RAM being replaced in computer systems where both programmability and data persistence are desired. One of ordinary skill would have been motivated at the time of applicants' invention to replace Dao's RAM with a programmable type of ROM to maintain programmability while improving data persistence under power conservation mode and/or to speed system recoverability, etc.

13. Claims 1, 5-9, 11-12, 15-16, and 18-19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Coon et al. (Patent No. 5,983,334).

14. The examiner would recommend applicants read col. 16, line 55 through col. 21, line 14 before responding.

15. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coon et al. (Patent No. 5,983,334).

16. Coon taught the invention substantially as claimed as in claim 15 including storing programmed code in firmware external to a processor which executes the

code, updating one or more registers associated with a logic unit in response to executing the programmed code, and controlling one or more functions of the logic unit based on a value stored in the one or more registers (col. 18, line 26 through col. 20, line 37). The examiner considers Coon's teaching of an external memory, such as RAM or the like, for storing microcode to be a teaching of firmware storing microcode. However, the examiner also takes Official Notice of the fact that advances in the art related to programmable read only memory such as EEPROM, flash memory, etc. have resulted in RAM and other forms of external memory being replaced in computer systems where both ready programmability and data persistence are desired. One of ordinary skill would have been motivated at the time of applicants' invention to replace Coon's RAM with a programmable type of ROM to maintain programmability while improving data persistence under power conservation mode and/or to speed system recoverability, etc.

17. As to claim 16, Coon taught the second logic unit (col. 20, lines 23-26) and control of one or more functions of the second logic unit based on one of the registers associated with the logic unit (col. 19, lines 29-61).

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

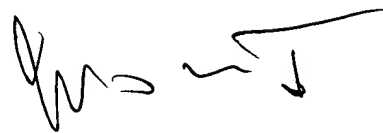
19. Agnew et al. (Patent No. 4,514,803).

20. Druke et al. (Patent No. 4,399,505).

21. Mahalingaiah et al. (Patent No. 6,141,740).

22. Any inquiry concerning this communication should be directed to William M.

Treat at telephone number (703) 305-9699.

A handwritten signature in black ink, appearing to read 'Wm M Treat', with a long horizontal line extending from the end.

**WILLIAM M. TREAT  
PRIMARY EXAMINER**